

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore®
 RELEASE 1.8

 Welcome
 United States Patent and
 Trademark Office

[Help](#) [FAQ](#) [Terms](#) [IEEE](#) [Quick Links](#)
[Peer Review](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

Your search matched **2** of **1131693** documents.
 A maximum of **500** results are displayed, **15** to a page,
 sorted by **Relevance** in **Descending** order.

Refine This Search:

You may refine your search by editing the current search expression or entering a new one in the text box.

(bist) <and> instantiating <and> memory

☐ Check to search within this result set
Results Key:

JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 ASIC BIST synthesis: a VHDL approach
Eberle, T.; McVay, B.; Meyers, C.; Moore, J.;

Test Conference, 1996. Proceedings., International , 20 Oct. 1996

Pages:741 - 750

[\[Abstract\]](#) [\[PDF Full-Text \(856 KB\)\]](#) **IEEE CNF**
2 Test and repair of large embedded DRAMs. 2
Nelson, E.; Dreibelbis, J.; McConnell, R.;

Test Conference, 2001. Proceedings. International , 30 Oct.-1 Nov. 2001

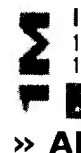
Pages:173 - 181

[\[Abstract\]](#) [\[PDF Full-Text \(785 KB\)\]](#) **IEEE CNF**
[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic](#)

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE



Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore®
RELEASE 1.8Welcome
United States Patent and
Trademark Office[Help](#) [FAQ](#) [Terms](#) [IEEE](#) [Quick Links](#)[Peer Review](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

Print Format

[Search Results](#) [[PDF FULL-TEXT 856 KB](#)] [NEXT](#) [DOWNLOAD C](#)Request Permissions
RIGHTSLINK®
COPYRIGHT CLEARANCE CENTER, INC.

ASIC BIST synthesis: a VHDL approach

[Eberle, T.](#) [McVay, B.](#) [Meyers, C.](#) [Moore, J.](#)

DFT Technol. Group, Sanders Associates Inc., Nashua, USA;

*This paper appears in: **Test Conference, 1996. Proceedings., International***

Meeting Date: 10/20/1996 - 10/25/1996

Publication Date: 20-25 Oct. 1996

Location: Washington, DC USA

On page(s): 741 - 750

Reference Cited: 8

Number of Pages: xii+951

Inspec Accession Number: 5526778

Abstract:

This paper describes the practical aspects of an automata design process and tool environment developed to rapidly effectively include **BIST** into ASIC designs. An overview **BIST** architecture is given describing **BIST** capabilities: mission logic, embedded and external **memory**, device interconnect **BIST** capability used to assist module/**BIST**. A high level synthesis approach is employed using VHDL language in a way unique to its intended purpose: automatic means for **instantiating** VHDL **BIST** structures.

an ASIC design is described. Other automated phases of the development cycle are discussed including testability enhancement of the ASIC core and test stimulus generation. Foundry, factory, and field test. Results are presented for ASIC designs ranging in gate count from 56 k-164 k gates (complexity from controllers to data processors)

Index Terms:

[SRAM chips](#) [application specific integrated circuits](#) [automatic equipment](#) [automatic testing](#) [built-in self test](#) [design for testability](#) [hardware description languages](#) [high level synthesis](#) [logic test](#) [production testing](#) [56 to 164 k](#) [ASIC BIST synthesis](#) [ASIC design](#) [ASIC mission logic](#) [BIST architecture](#) [SRAM](#) [VHDL language](#) [automated design](#) [controllers](#) [data processors](#) [embedded memory](#) [external memory](#) [factory testing](#) [field test](#) [foundry](#) [high level synthesis](#) [interconnect BIST](#) [module/PCB BIST](#) [test stimulus generation](#)

Documents that cite this document

There are no citing documents available in IEEE Xplore at this time.

[Search Results](#) [\[PDF FULL-TEXT 856 KB\]](#) [NEXT](#) [DOWNLOAD CITATION](#)

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved